



### Features

- Eight channels of ESD protection
  - Note: For 2 and 4 channel devices, see the CM1293A datasheet.
- Provides ESD protection to IEC61000-4-2
  - $\pm 8\text{kV}$  contact discharge
- Low loading capacitance of 2.0pF max.
- Low clamping voltage
- Channel I/O to I/O capacitance 1.5pF typical
- Zener diode protects supply rail and eliminates the need for external by-pass capacitors
- Each I/O pin can withstand over 1000 ESD strikes\*
- Available in MSOP, lead-free packaging

### Applications

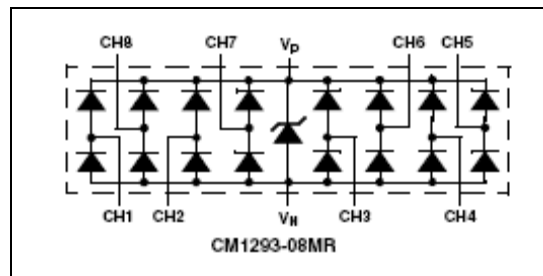
- DVI ports, HDMI ports in notebooks, set top boxes, digital TVs, LCD displays
- Serial ATA ports in desktop PCs and hard disk drives
- PCI Express ports
- General purpose high-speed data line ESD protection

### Product Description

The CM1293 family of diode arrays has been designed to provide ESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive ( $V_P$ ) or negative ( $V_N$ ) supply rail. A Zener diode is embedded between  $V_P$  and  $V_N$ , offering two advantages. First, it protects the  $V_{CC}$  rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1293 will protect against ESD pulses up to ( $8\text{kV}$  contact discharge) per the IEC 61000-4-2 Level 4 standard.

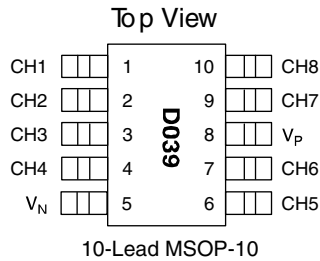
This device is particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

### Block Diagram



\*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to  $\pm 8\text{kV}$  contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

**PACKAGE / PINOUT DIAGRAMS**



Note: This drawing is not to scale.

**PIN DESCRIPTIONS**

**8-CHANNEL, 10-LEAD MSOP-10 PACKAGE**

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	CH3	I/O	ESD Channel
4	CH4	I/O	ESD Channel
5	V <sub>N</sub>	GND	Negative voltage supply rail
6	CH5	I/O	ESD Channel
7	CH6	I/O	ESD Channel
8	V <sub>P</sub>	PWR	Positive voltage supply rail
9	CH7	I/O	ESD Channel
10	CH8	I/O	ESD Channel

CM1293

## Ordering Information

PART NUMBERING INFORMATION				
			Lead-free Finish	
# of Channels	Leads	Package	Ordering Part Number <sup>1</sup>	Part Marking
8	10	MSOP-10	CM1293-08MR	D039

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

## Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
Operating Supply Voltage ( $V_p - V_N$ )	6.0	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	$(V_N - 0.5)$ to $(V_p + 0.5)$	V

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C
Package Power Rating MSOP-10 Package (CM1293-08MR)	400	mW

**ELECTRICAL OPERATING CHARACTERISTICS** (SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_P$	Operating Supply Voltage ( $V_P-V_N$ )			3.3	5.5	V
$I_P$	Operating Supply Current	$(V_P-V_N)=3.3V$			8.0	$\mu A$
$V_F$	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 8mA$ ; $T_A=25^\circ C$	0.60 0.60	0.80 0.80	0.95 0.95	V V
$I_{LEAK}$	Channel Leakage Current	$T_A=25^\circ C$ ; $V_P=5V$ , $V_N=0V$		$\pm 0.1$	$\pm 1.0$	$\mu A$
$C_{IN}$	Channel Input Capacitance	At 1 MHz, $V_P=3.3V$ , $V_N=0V$ , $V_{IN}=1.65V$		1.0	1.5	pF
$\Delta C_{IN}$	Channel Input Capacitance Matching	At 1 MHz, $V_P=3.3V$ , $V_N=0V$ , $V_{IN}=1.65V$		0.02		pF
$C_{MUTUAL}$	Mutual Capacitance between signal pin and adjacent signal pin	At 1 MHz, $V_P=3.3V$ , $V_N=0V$ , $V_{IN}=1.65V$		0.11		pF
$V_{ESD}$	ESD Protection Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000-4-2 standard	Notes 3 and 4; $T_A=25^\circ C$		$\pm 8$		kV
$V_{CL}$	Channel Clamp Voltage Positive Transients Negative Transients	$T_A=25^\circ C$ , $I_{PP} = 1A$ , $t_p = 8/20\mu s$ ; Notes 4		+8.8 -1.4		V V
$R_{DYN}$	Dynamic Resistance Positive Transients Negative Transients	$I_{PP} = 1A$ , $t_p = 8/20\mu s$ Any I/O pin to Ground; Note 4		0.7 0.4		$\Omega$ $\Omega$

Note 1: All parameters specified at  $T_A = -40^\circ C$  to  $+85^\circ C$  unless otherwise noted.

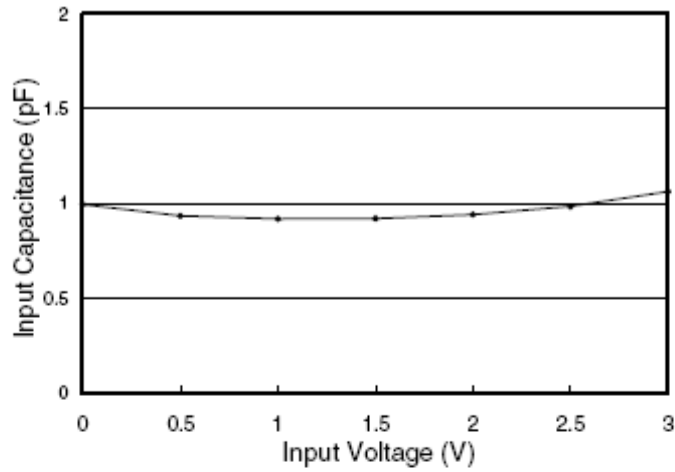
Note 2: Human Body Model per MIL-STD-883, Method 3015,  $C_{Discharge} = 100pF$ ,  $R_{Discharge} = 1.5K\Omega$ ,  $V_P = 3.3V$ ,  $V_N$  grounded.

Note 3: Standard IEC 61000-4-2 with  $C_{Discharge} = 150pF$ ,  $R_{Discharge} = 330\Omega$ ,  $V_P = 3.3V$ ,  $V_N$  grounded.

Note 4: These measurements performed with no external capacitor on  $V_P$  ( $V_P$  floating).

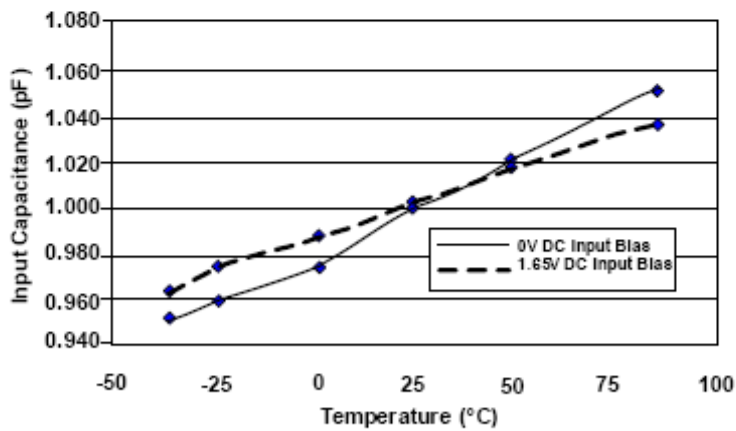
## Performance Information

### Input Channel Capacitance Performance Curves



**Typical Variation of C<sub>IN</sub> vs. V<sub>IN</sub>**

(f=1MHz, V<sub>P</sub> = 3.3V, V<sub>N</sub> = 0V, 0.1 μF chip capacitor between V<sub>P</sub> and V<sub>N</sub>, 25°C)



**Typical Variation of C<sub>IN</sub> vs. Temp**

(f=1MHz, V<sub>IN</sub>=30mV, V<sub>P</sub> = 3.3V, V<sub>N</sub> = 0V,  
0.1 μF chip capacitor between V<sub>P</sub> and V<sub>N</sub>)

## Performance Information (cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

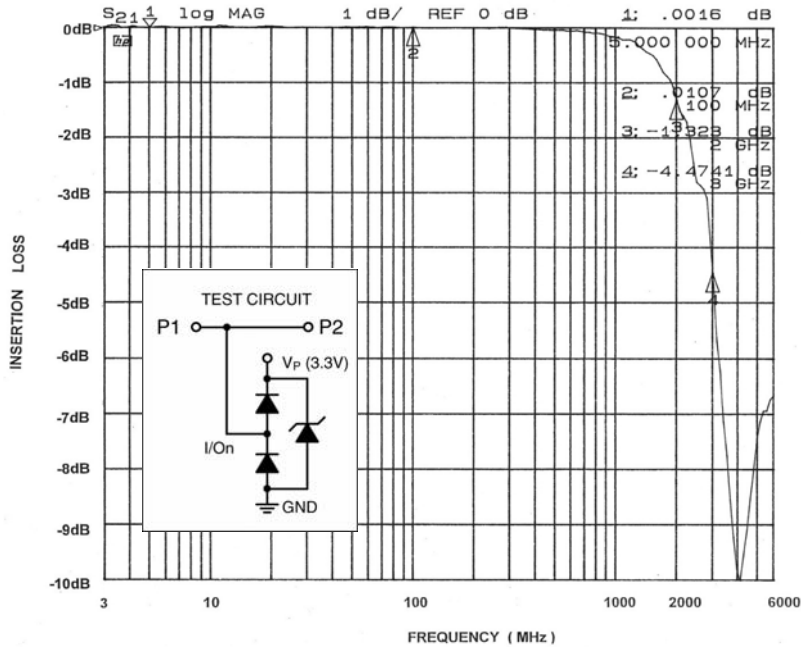


Figure 1. Insertion Loss (S21) VS. Frequency (0V DC Bias,  $V_p=3.3V$ )

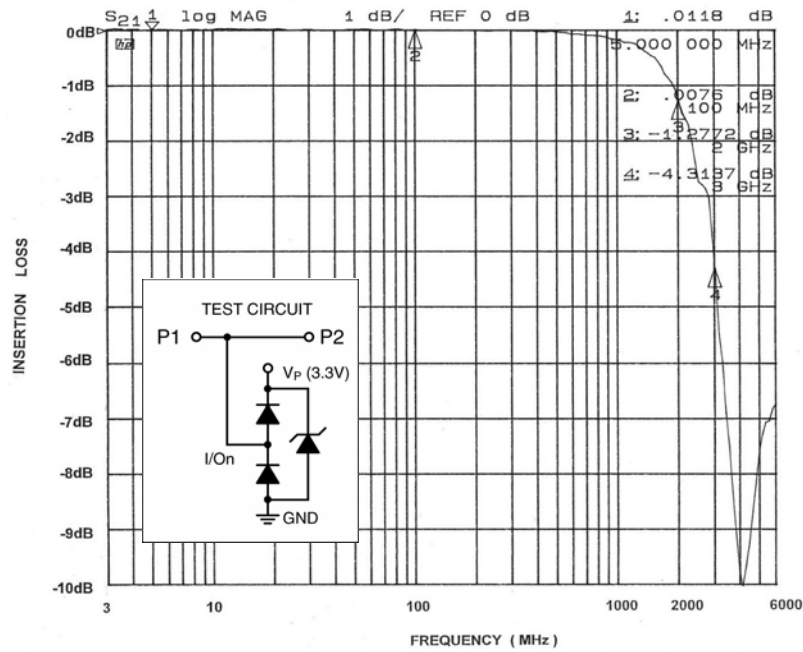


Figure 2. Insertion Loss (S21) VS. Frequency (2.5V DC Bias,  $V_p=3.3V$ )

## Application Information

### Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Application of Positive ESD Pulse between Input Channel and Ground, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by  $L_1$  and  $L_2$ . The voltage  $V_{CL}$  on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where  $I_{ESD}$  is the ESD current pulse, and  $V_{SUPPLY}$  is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here  $d(I_{ESD})/dt$  can be approximated by  $\Delta I_{ESD} / \Delta t$ , or  $30 / (1 \times 10^{-9})$ . So just 10nH of series inductance ( $L_1$  and  $L_2$  combined) will lead to a 300V increment in  $V_{CL}$ !

Similarly for negative ESD pulses, parasitic series inductance from the  $V_N$  pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1293 has an integrated Zener diode between  $V_P$  and  $V_N$ . This greatly reduces the effect of supply rail inductance  $L_2$  on  $V_{CL}$  by clamping  $V_P$  at the breakdown voltage of the Zener diode. However, for the lowest possible  $V_{CL}$ , especially when  $V_P$  is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22 $\mu$ F ceramic chip capacitor be connected between  $V_P$  and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the  $V_P$  pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

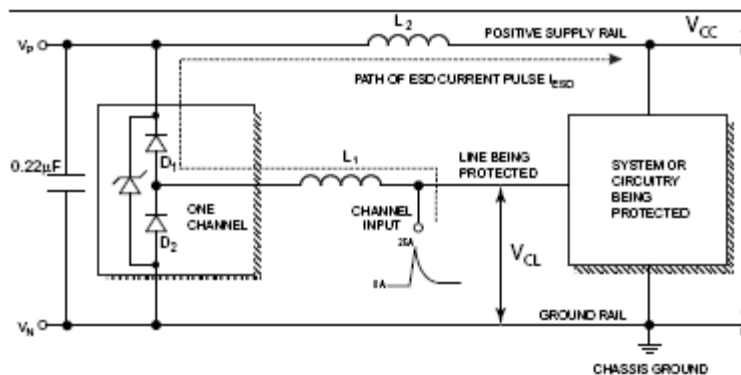


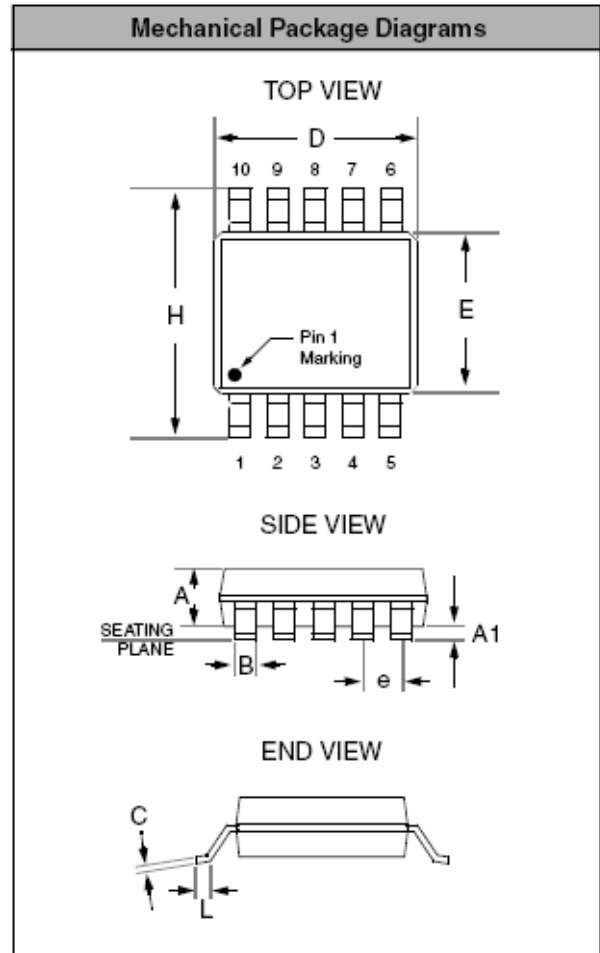
Figure 3. Application of Positive ESD Pulse between Input Channel and Ground

## Mechanical Details

### MSOP-10 Mechanical Specifications, 10 pin

The 10-pin MSOP package dimensions are presented below.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	10			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	0.75	0.95	0.028	0.038
A1	0.05	0.15	0.002	0.006
B	0.17	0.27	0.007	0.013
C	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.0196 BSC	
H	4.90 BSC		0.193 BSC	
L	0.40	0.70	0.0137	0.029
# per tape and reel	4000			
Controlling dimension: millimeters				



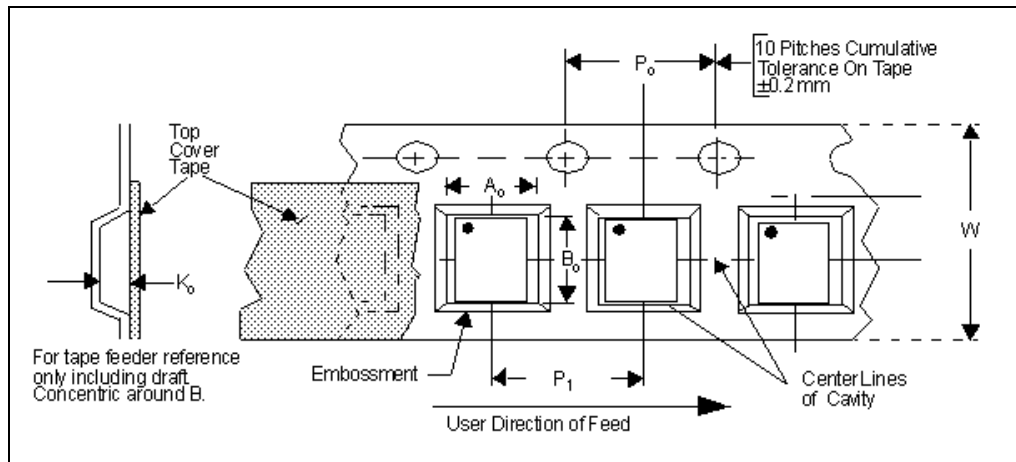
Package Dimensions for MSOP-10




# CM1293

## Tape and Reel Specifications

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) $B_0 \times A_0 \times K_0$	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	$P_0$	$P_1$
CM1293-08MR	3.00 X 3.00 X 0.85	3.30 X 5.30 X 1.30	12mm	330mm (13")	4000	4mm	4mm



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